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12-12-02

Attorney Docket No: RAL9990056/1474P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Bullis et al.

Serial No. 09/409,940 Group Art Unit: 2123

Filed: September 30, 1999 Examiner: Ferris III, F.

For: METHOD AND SYSTEM FOR PROVIDING HIERARCHICAL SELF-CHECKING IN ASIC SIMULATION

Assistant Commissioner for Patents
Washington, D.C. 20231

DECLARATION UNDER 37 C.F.R. 1.132

I, Raj Singh, hereby declare that:

1. I am the inventor of the subject matter recited in the claims of the above-identified application.
2. I have reviewed the specification of the present applications as well as Figure 1 attached as Exhibit A.
3. It is my opinion that one of ordinary skill in the art will readily understand that the method and system in accordance with the present invention, as disclosed in the present application, are based on inter-process communication between the units under test (islands), embodiments of the system and method in accordance with the present cas

(models) and the test case. The islands reside in the test bench during use of the models. The models are described in the specification as the snooper, checker and generator.

4. It is my opinion that based upon reading the specification of the present application, one of ordinary skill in the art would readily realize that each snooper, checker and generator can be considered to include a physical portion and a logical portion, which is termed the intelligence in the specification. The physical portion includes interfaces and a mechanism for controlling the interfaces. The interfaces of the model couple to the interface of the island. It is my opinion that one of ordinary skill in the art would readily recognize that the interfaces typically include I/O ports for connecting to the island and a process for controlling the I/O ports that operates in system-clock domain where simulation time is advanced.

5. As described in the specification, the intelligence of the snooper, checker and generator can be implemented using a number of languages. In one embodiment, the intelligence of the snooper, checker and generator function as follows. As described in the specification, the test case provides data and a framework for the generator. The test case thus requests the generator to perform a particular simulation of the island and provides data for the simulation. It is my opinion that one of ordinary skill in the art will readily recognize that in requesting that the generator perform a particular simulation, the test case calls functions provided by, or procedures contained in, the intelligence of the generator. Thus, the intelligence required in the test case is minimal. It is also my opinion that one of ordinary skill in the art will also recognize that the intelligence of the generator helps

carry out the desired procedures called by the test case, including providing the appropriate and preferably randomized inputs to the island in response to a request for service from the test case. The intelligence of the generator also uses the data provided by the test case to generate these inputs.

6. The intelligence of the snooper and checker preferably causes the snooper and checker to wait in loops for outputs to be provided from the island. The intelligence of the snooper and checker also obtain the outputs from the interfaces (the physical portion) and check the outputs against desired outputs. As described in the specification, the intelligence of the checker can also generate the desired outputs.

7. Thus, the intelligence of the snooper, checker and generator can be viewed as providing internal data structure (buffering and queuing) and a process for manipulating these data structures in response to service request by other models and test case via a set of procedure calls and global signals. The physical and logical parts of each snooper, checker and generator communicate with each other via a set of internal signals. In one embodiment, the logical part operates in simulator's delta-time domain.

8. One embodiment of the method and system in accordance with present invention as recited in varying scope in the claims of the present application was successfully applied in design of a Common ATM Data mover (CAD) processor chip. Other embodiments of the method and system in accordance with the present invention have been since applied in several other ASIC designs. Consequently, the functions of the snooper, checker and generator can also be understood in conjunction with the embodiment used in the

development of the CAD processor chip.

9. Figure 1, attached hereto as Exhibit A, shows a full-chip simulation environment for the CAD ASIC with which one embodiment of the present invention was used. The ASIC was designed in a hierarchical fashion and was recursively broken into logic islands of varying sizes. At the highest level, the CAD ASIC is broken into two islands, namely CAD-UP and CAD-DN. The CAD-UP island is subsequently decomposed into five smaller logic islands, namely PIF-UP, RAM, CAD-UP core, SDM-UP, and SIF-UP. Each island is verified separately in its own test bench environment with a set of snooper, checker, and generator models. As the logic islands are integrated together, some of the generator models on external interfaces are replaced by the actual logic island providing the stimulus on now the internal interface. Also some of the checker models on external interfaces in the smaller island environment are replaced by a snooper on the same interface that becomes an internal interface in the bigger island in the next level of hierarchy. However, as can be seen, many of the original snoopers, checkers, and generators continue to be used as-is (providing incremental checking) in the new environment demonstrating the re-use of the simulation models.

10. Figure 1 also depicts various snoopers, checkers, and generators connected to various islands. The lines with arrows between models and between models and test case represent the direction of information exchange. The information generated by a model can be predicated on information received from multiple other models in the test bench.

11. The use of the **UTOPIA_TX** generator and associated snooper and checker in testing the

PIF-UP island is described to illustrate the interactions among test case, generator, checker, and snooper. The test case proceeds with a request to **UTOPIA_TX** generator to send ATM cells (including one RM cell) with specified cell parameters passed through the procedure call interface. In this case, therefore, the simulation requested checks the transmission of, receipt of and expected data related to the ATM cells. Thus, the test case calls the procedure contained in the generator used to send ATM cells. The **UTOPIA_TX** generator model sends the cell over the physical interface as well as broadcast it over the global signal **utop_cell_out** with a trigger **utop_cell_xmit**. The **PIFUPCHK** checker monitors the **utop_cell_xmit** trigger signal and buffers the expected data. It later compares it against the response data gathered from **EGL_ANALYZER_UP** snooper in the manner described above.

12. In addition, Table 1, attached hereto as Exhibit B, indicates the file names of procedures used to implement the intelligence of various embodiments of the models used in developing the CAD ASIC described above and shown in Figure 1 of Exhibit A.

13. The ***_e.vhd** entity files represent the physical I/O interface of a model. In some cases a checker may not have any physical interface. The ***_a.vhd** architecture files contain the processes which are sensitive to either I/O port signals or global signals of a model.

14. The ***_p.vhd** package files contain declaration of constants, shared variables, global signals, procedure and function interfaces. The ***_pb.vhd** package-body files contain the definitions of procedures and function in the corresponding package. The procedures and functions of a model are called by a test case or other models to request a service, such as

asserting stimulus on model's I/O interfaces using the values of the arguments of the procedure call. The global signals are used to broadcast data to be exchanged between models without a physical bus or interconnect between them. This is the mechanism used by a generator to send out-of-band expected response data of a island to a stimulus applied by the generator on the external input interface of the island, and by a snooper to provide the island response observed on the external output interface of the island to a checker to perform a dynamic compare for correctness. These data exchanges are denoted by the lines with arrows in the **Error! Reference source not found.**.

15. The ***_tb.vhd** test bench file instantiates the island along with all other necessary generators, snoopers, and checkers. The corresponding ***_tb_c.vhd** configuration file allows multiple modes of simulation , such as rtl or gates, to be specified.

16. The **pif_pid0.vhd** test case instantiates the test bench entity **TOP_PIF_UP**. The process in the architecture section of the test case calls on **MBUS_TX** generator model to send a packet or cell into the **PIF_UP** island. The **MBUS_TX** generator sends the cell over the physical interface as well as broadcast the cell data on global signal **mbus_cell_out** with associated trigger **mbus_cell_xmit**. The **PIFUPCHK** checker monitors the **mbus_cell_xmit** trigger signal and buffers the **mbus_cell_out** data. The **PIFUPCHK** also monitors the global trigger **segl_write_trigger** from **EGL_ANALYZER_UP** snooper and compares the response data **segl_from_data** with **mbus_cell_out**.

17. Thus, upon reading the specification, it is my opinion that one of ordinary skill in the art will realize that the procedures and functions of a model are called by a test case or other

models to request a service, such as asserting stimulus on model's I/O interfaces using the values of the arguments of the procedure call. The procedures and functions are called by the test case requesting service of a generator. The global signals are used to broadcast data to be exchanged between models without a physical bus or interconnect between them. This is the mechanism used by a generator to send out-of-band expected response data of a island to a stimulus applied by the generator on the external input interface of the island, and by a snooper to provide the island response observed on the external output interface of the island to a checker to perform a dynamic compare for correctness. These data exchanges are denoted by the lines with arrows in Figure 1.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Raj Singh

12/2/2002

Date

Exhibit A

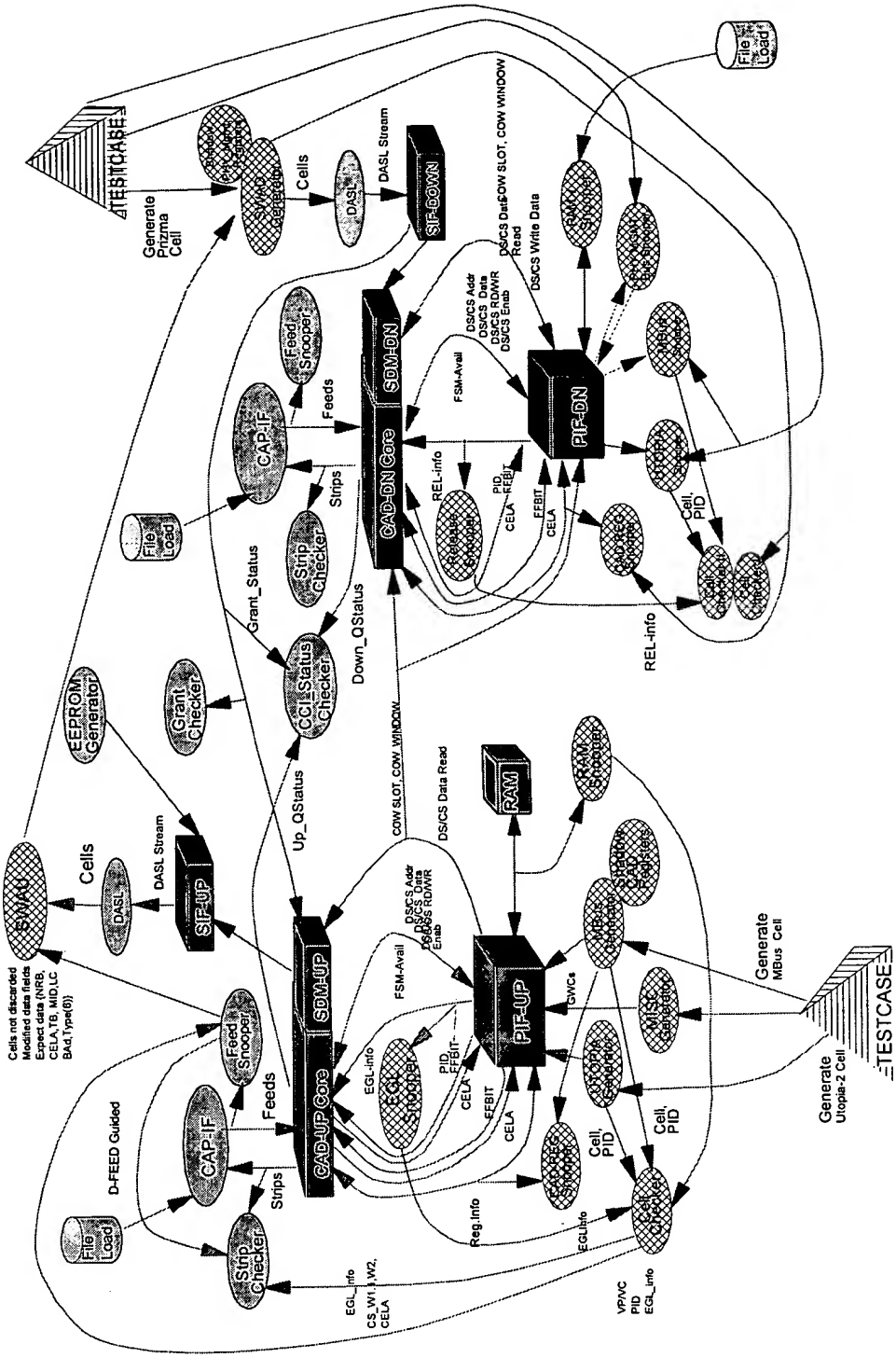

Exhibit B

Table 1:Sample Components of PIF-UP Island Simulation Environment

Entity Type	Entity Name	Associated File Names
Test bench	TOP_PIF_UP	pif_up_tb.vhd pif_up_tb_c.vhd
Test case	PIF_PID0	pif_pid0.vhd
Generator model	MBUS_TX	mbus_tx_e.vhd mbus_tx_e.vhd mbus_tx_p.vhd mbus_tx_pb.vhd
Generator model	UTOPIA_TX	utopia_tx_e.vhd utopia_tx_a.vhd utopia_tx_p.vhd utopia_tx_pb.vhd
Snooper model	EGL_ANALYZER_UP	egl_analyzer_up_e.vhd egl_analyzer_up_p.vhd egl_analyzer_up_a.vhd
Checker model	PIFUPCHK	piupchk_e.vhd pifupchk_a.vhd pifupchk_p.vhd pifupchk_pb.vhd